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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	Paul F. Struhsaker, et al.
Serial No.	:	09/839,509
Filed	:	April 20, 2001
For	:	BACKPLANE ARCHITECTURE FOR USE IN WIRELESS AND WIRELINE ACCESS SYSTEMS
Group No.	:	2616
Examiner	:	Ian N. Moore

MAIL STOP APPEAL BRIEF - PATENTS
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Sir:

APPELLANTS' SUPPLEMENTAL REPLY BRIEF

This Supplemental Reply Brief is responsive to the remand from the Board of Patent Appeals and Interferences and to the Examiner's Supplemental Answer mailed March 29, 2007. Please charge any additional necessary fees to Deposit Account No. 50-0208.

ARGUMENT

1. The rejection of claims 10–13 and 17 under 35 U.S.C. § 102(e) as being anticipated by *Dove*.

a. The recited serial link(s) are not found in the cited reference.

As previously noted, independent claim 10 recites that the high tier bus comprises one or more serial links. The final rejection cites cell bus 550 in *Dove* as satisfying the limitation. However, cell bus 550 includes eight parallel bits or signal lines, and is therefore a parallel bus. *Dove*, column 4, lines 24–27, column 7, lines 47–48.

The Examiner's Answer adopts the position that each individual signal line may be considered a "serial link":

> Dove discloses one or more serial links (see FIG. 5, **each cell bus/link 550 transmits cells serially between one end point CBI_1 520 to another end point $CBI_{(1)}$ 510, thus, each link/bus is a point-to-point serial link, and there are "n" link/bus 550**) that is capable of aggregate traffic rates of up to approximately twenty gigabits per second (**see col. 4, lines 24-30; see col. 5, lines 16-20, 26-34, see col. 6, lines 10-19; see col. 7, line 4-65**).
>
> Also, it is clear to one skilled in the ordinary art that very basic and fundamental concept of transmitting data (**see Dove FIG. 5, data**) from one end point (**see Dove FIG. 5, CBI_1 520**) to the other end point (**see Dove FIG. 5, $CBI_{(1)}$ 510**) over a signal link/bus (**see Dove FIG. 5, a link/bus 550**), the data must be send in **serial, sequential order, or one after another** (see Dove FIG. 5 below). Thus, Dove's link/bus 550 is a serial link/bus that performs data transmission in a serial, sequential order, or point-to-point since there is no other way to send data in a point-to-point connection with a single line/bus. Again, Dove discloses the "functionality" of "serial" transmission by showing a single link/bus 550 that connects between two points and performs serial/sequential transmission since one skill in the ordinary art would clearly understand well established basic point-to-point transmission concept where data must be send in serial or sequential order.

Examiner's Answer, page 13 (emphasis in original). This reasoning is fundamentally flawed. The overall structure in *Dove* may not be artificially dissected as proposed in the Examiner's Answer merely for the purposes of finding anticipation. The fact that a portion of a parallel interface may, if one squints one's eyes and holds one's tongue *just so*, be seen to have characteristics similar to those of a serial interface does NOT make the parallel interface a serial interface.

The concept of a serial link or interface is understood by those of ordinary skill in the art:

> **serial interface** [COMPUT SCI] A link between a microcomputer and a peripheral device in which data is transmitted over a single conductor, one bit at a time. Also known as a serial port.

McGraw-Hill Dictionary of Scientific and Technical Terms (6th ed. 2003), page 1902 (copy attached). The cited structure of *Dove* (i.e., link 550 between CBI_1 520 and $CBI_{(1)}$ 520) does NOT include just a single conductor, or transmit data one bit at a time. The structure depicted in FIG. 5 of *Dove* includes a diagonal slash through the line representing link 550:

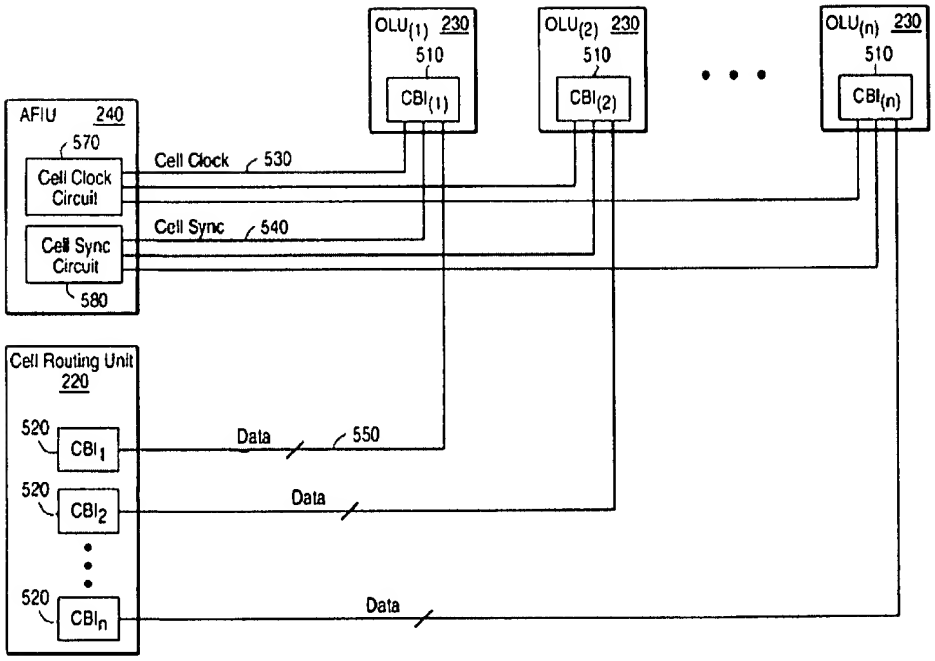

FIG_5

That slash indicates that the line represents multiple conductors (and is often accompanied by a number reflecting the number of conductors represented). *Dove* states that the data path for link 550 is eight bits (one byte) wide, made up of signal lines number "0" through "7" (indicated by the reference to "Tx_Data[7:0]" and "Rx_Data[7:0]"):

> For the cell bus embodiment shown in FIG. **5**, the cell bus data path width is byte wide and symmetrical (i.e., transmit data "Tx_Data" and receive data "Rx_Data" on transported the data lines **550**). . . . .
> Table 1 further describes the signals of the cell bus for the embodiment of FIG. 5.

TABLE 1

Signal	Description	Source	Logic Level	Value Range
Cell Clock	CBI clock	AFIU	DPECL	25 MHZ
Cell Sync	Master Cell Sync	AFIU	GTL	68 clocks
Tx_Data[7:0]	Tx Data byte	CRU	GTL	D0-D67
RxData[7:0]	Rx Data byte	OLU	GTL	D0-D67

Dove, column 7, lines 47–50, column 8, lines 19–29. Thus, even if the artificial dissection of the cited structure in *Dove* proposed in the Examiner's Answer were proper, the argument fails because each link 550 is made up of eight parallel conductors and transmits one byte of data at a time, not a single data bit at a time on a single conductor.

The Examiner's Answer further states:

> Second, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (**i.e., excluding cell-based buses, bitwise or cells (53 bytes) of data concurrently**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims . . . . Thus, it is irrelevant to argue the limitation that is not being claimed.

Examiner's Answer, page 14 (emphasis in original). However, the limitations dismissed as "irrelevant" are, in fact, recited within the rejected claim(s). The claims recite a "serial link." As noted above, the customary and accepted meaning of the term "serial link" is a link in which data is transmitted over a single conductor, one bit at a time. Such a meaning necessarily excludes cell-based buses and/or transmitting a byte (or 53 bytes) of data concurrently. Where the ordinary meaning of a claim term incorporates the limitations, there is no need to explicitly (and redundantly) recite those limitations within the claims.

The Examiner's Answer further states:

> Third, examiner's interpretation of "serial link" neither contrary to specification nor ordinary and accepted meaning of the term since both applicant's serial bus/link 415 (see applicant FIG. 4) and Dove's serial link/bus 550 (see Dove's FIG. 5) are identical and performed identical functionality as shown below.

Examiner's Answer, page 14. As noted above, the "ordinary and accepted meaning" of the term "serial link" is, in fact, contrary to the Examiner's bizarre and contorted interpretation necessitating artificial dissection of structures within the cited reference. As also noted above, even with the artificial dissection of structures, the link 550 in Figure 5 of *Dove* is not "serial," but is instead a byte-wide link.

b. The recited at least two serial links are not found in the cited reference.

As previously noted, dependent claim 17 recites that the backplane comprises at least two high speed serial links for each interface control processor slot in the backplane, which the final rejection are satisfied by cell clock 530 and cell sync 540 within Figure 5 of *Dove*. The Examiner's Answer states:

> Dove discloses at least two (2) high speed serial links (**see FIG. 5, Cell clock 520 and cell sync 540 between AFIU 240 and OLU 230; see FIG. 10, links between LIU 230 and ABIUs**) for each interface control processor slot (**see FIG. 5 and FIG. 2, AFIU 240**) in said backplane (**see col. 6, lines 5-67; see col. 5, lines 35-55; see col. 12, lines 12-30; see col. 7, line 15-21,33-37**) as shown below.

Examiner's Answer, page 16 (emphasis in original). As noted above, the customary and accepted meaning of the term "serial link" is a link in which data is transmitted over a single conductor, one bit at a time. Cell clock 520 and cell sync 540 signals transmit control signals (i.e., a clock signal and a sync signal), not data. Similarly, the signals between ABIU 240 and line unit 230 in Figure 10 of *Dove* are clock signals, not data signals. *Dove*, column 12, lines 12–13 ("FIG. 10 is a block diagram illustrating one embodiment for clock distribution in the cell bus.").

2. The rejection of claims 1–4, 7–8 and 20 under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al.*

As previously noted, independent claims 1 and 20 each recite that the low tier comprises a cell-based bus capable of lower aggregate traffic rates (up to approximately two gigabits per second), while the high tier comprises one or more serial links capable of higher aggregate traffic rates (up to approximately twenty gigabits per second). *Manchester et al*, cited in the final rejection as satisfying these limitations, teaches exactly the opposite: a low-speed time division multiplexed (TDM) bus 70 comprising point-to-point serial links and a high-speed ATM (cell-based) bus 72. *Manchester et al*, column 8, lines 19–47. *Manchester et al* specifically states that the traffic rates on TDM bus 70 are slower than those on ATM bus 72.

The Examiner's Answer relies on high speed ATM (HSA) bus 72 in *Manchester et al* and large cell switch 1100 in *Tabu et al* as satisfying the recited one or more serial links capable of higher aggregate traffic rates. As previously noted, the ordinary and accepted meaning of "serial link" necessarily excludes parallel or cell-based buses such as HSA bus 72 in *Manchester et al* and large cell switch 1100 in *Tabu et al.*

The Examiner's Answer also asserts that the language reciting "capable of" in the claim renders the limitation "optional." Examiner's Answer, page 20. This is an incorrect statement of the applicable law. Claim language such as "capable of" (or "adapted to") may not be ignored where the clause states a condition material to patentability, rather than merely an intended result of a process step. MPEP § 2111.04, page 2100-55 (8th ed. rev. 4 October 2005). The claims in the

present application recite that the structures defined are "capable of aggregate traffic rates of up to approximately two gigabits per second" and "capable of aggregate traffic rates of up to approximately twenty gigabits per second." These limitations are in no way "optional," but instead impose affirmative conditions on the claimed subject matter. Structures incapable of the aggregate traffic rates listed – including those in the cited references – are not encompassed by the claim language.

3. The rejection of claim 5 under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of *Chui et al.*

As previously noted, claim 5 recites that ATM cells are wrapped with a header to allow circuit board switching based on a connection map, while the portion of *Chiu et al* cited in the final rejection teaches that the header depicted in Figure 9 is NOT used for circuit board level switching of ATM cells, but instead only for cell bus traffic and multicast traffic.

The Examiner's Answer states:

> Chui discloses a lower tier bus (**see FIG. 9, ATM cell is encapsulated with cell bus header byte; see col. 8, lines 1-6**) to allow to said lower tier bus to switch cell based traffic according to the connection map (**see FIG. 24-25, connection address map RAM data; or see FIG. 14, RAM 1416**) on each circuit board card (**see FIG. 6; cards 606-608,610-612**) connected to said low tier bus (**see col. 5, lines 60 to col. 6, lines 67; see col. 8, line 47-48; see col. 14, lines 30–65**).
>
> Chui's FIG. 9 discloses a cell format (which utilizes by cell bus in FIG. 6) comprising a cell bus header which wraps/encapsulates ATM cells. Moreover, a cell format (defined in FIG. 9) is switched in the cell bus according to address map RAM look-up logic in order to determine where the target/destination service modules and perform switching accordingly. Chui discloses in col. 8, lines 43-44, 48-53:
>
> "For ATM traffic . . . . **the ECP performs cell bus interface polling address to target address mapping** using thirty-two

> possible polling address destinations that are mapped to twenty-six targets. **The mapping is performed by Address Map RAM 1416 look-up logic**, wherein the targets are the service modules via a CBM, a second PSM Card via a CBS, and a MCE..." (Emphasis added)
>
> Thus, it is clear that Chui discloses the target/destination address map lookup is performed for ATM encapsulated bus cell format (defined in FIG. 9) switching.

Examiner's Answer, page 23 (emphasis in original). In should first be noted that the selective cutting of text from the *Chiu et al* in the Examiner's Answer changes the meaning of the language quoted. Read in context, *Chiu et al* actually teaches that ATM cells are simply forwarded by the Egress Cell Processor (ECP) to a Cell Bus Slave (CBS) without (emphasis supplied below to text omitted from quotation within Examiner's Answer):

> For ATM traffic, *the ECP simply forwards the cell to the CBS, without the Cell Bus Header look-up. The ECP unloads cells from the ECIC input FIFOs and checks the parity of the data read from these FIFOs.*
>
> The ECP performs cell bus interface polling address to target address mapping using thirty-two possible polling address destinations that are mapped to twenty-six targets. The mapping is performed by Address Map RAM 1416 look-up logic, wherein the targets are the service modules via a CBM, a second PSM Card via a CBS, and a MCE.

Chiu et al, column 8, lines 43–53. Thus, contrary to the assertion in the Examiner's Answer, *Chiu et al* actually teaches that the Cell Bus Header look-up is NOT performed for ATM traffic.

Regardless, the claim requires that the ATM cell be wrapped within a enabling circuit board switching of the ATM packets. Such a feature is not suggested by *Chiu et al.* The Examiner's Answer confuses use of a connection map generally (e.g., by software switching) with board switching (i.e., by hardware), specifically.

4. The rejection of claim 6 under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of *Lentz et al.*

As previously noted, claim 6 recites two parallel buses each having a 32-bit data path in the low tier, which the final rejection asserts in obvious based on the mere existence of such data paths in the prior art, without any motivation or incentive.

In asserting that the claims are obvious, the Examiner's Answer proposes a motivation or incentive for combining the single 32-bit data path of *Lentz et al* with the proposed combination of structures from *Manchester et al* and *Tabu et al* as follows:

> In this case, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide 32 bit data bus, as taught by Lentz, in the combined system of Manchester and Tabu, so that it would provide a flexible frame word for low end products; see Lentz col. 2, line 5-40.

Examiner's Answer, page 24. The cited portion of *Lentz et al* reads:

> The present invention provides a memory system interface design for a processor and a method of operating such an interface which provides access to a dual width memory bus. Specifically, the present invention provides a mechanism that allows a computer-based system to access either a 32 bit memory bus or a 64 bit memory bus. The 32 bit memory bus would be used for low-end products, while the 64 bit memory bus would be used for high-end products. A memory control unit (MCU) of the present invention supports both modes: the 32 bit bus mode and the 64 bit bus mode. The present invention in one embodiment has been integrated onto a microprocessor chip.
>
> Selecting a 32 bit or 64 bit memory subsystem provides a user with a flexible framework in which to design a system. The user can adjust system cost and performance by choosing to utilize a 32 bit or 64 bit external bus. The present invention provides a system and method which decreases the amount of wires necessary to transfer data. Moreover, a microprocessor chip incorporating the present invention allows switching between the 32 bit or 64 bit external memory bus without changing the control signals and/or system configuration.

> The present invention provides a computer-based system and method for efficiently transferring data over an external memory bus between a main memory and a bus requestor, comprising a dual width memory subsystem configured to provide access to a plurality of different external memory buses. The dual width memory subsystem comprises a plurality of multiplexers connected to receive data from the bus requestor and a storage device connected to receive and store data from the plurality of multiplexers, the data is stored in blocks depending on the width of the external bus. Furthermore, the dual width memory subsystem comprises a storage device connected to receive and store data from the external memory bus, the data is stored in blocks depending on the width of the external bus. A plurality of multiplexers connected to receive data from the storage device, and connected to send said data to a bus requestor in blocks determined by the limitations of the system.

Lentz et al, column 2, lines 3–42. Nothing in the cited portion of *Lentz et al* suggests that the ability to "provide a flexible frame word for low end products" derives specifically from the presence of the 32-bit data path alone; in fact, *Lentz et al* teaches that the presence of both 32-bit and 64-bit data paths is required.

Lentz et al, it should be noted, does not even relate to ATM or cell-based buses, and therefore cannot be said to motivate the use of 32-bit ATM or cell-based data paths in a low tier ATM bus according to the proposed combination of *Manchester et al* and *Tabu et al*.

Moreover, nothing in *Lentz et al* suggests specifically including two 32-bit data paths – rather than, say, one 32-bit data path and one 64-bit data path – in a low tier ATM bus according to the proposed combination of *Manchester et al* and *Tabu et al*.

5. The rejection of claim 9 under 35 U.S.C. § 103(a) as being unpatentable over *Manchester et al* in view of *Tabu et al* and further in view of *Pajowski et al.*

As previously noted, claim 9 recites providing a redundant clock reference for the low tier. Nothing in either over *Manchester et al* or *Tabu et al* suggests that timing errors in (asynchronous) ATM buses of the type disclosed therein are such a problem as to motivate one skilled in the art to look to clock redundancy for synchronous systems as disclosed in *Pajowski et al.*

The Examiner's Answer asserts that clock signals are employed in asynchronous systems as well as synchronous systems, introducing additional prior art for the first time to support that contention. Examiner's Answer, pages 25–26. However, the Examiner's Answer completely misses the point. While clock signals may indeed be employed in asynchronous systems, nothing in the cited art suggests that timing errors relating to such clock signals in asynchronous systems are at all problematic. The only evidence of timing errors comes from *Pajowski et al*, which discloses a synchronous rather than asynchronous system. Because there is no evidence of egregious timing errors in asynchronous systems, no motivation exists for one skilled in the art to look for a solution to such timing error problems anywhere, including particularly solutions employed for synchronous systems.

6. The rejection of claims 14–16 under 35 U.S.C. § 103(a) as being unpatentable over *Dove*.

As previously noted, claim 14 recites that the serial links operate at the same clock rate as the back plane, while the cited portions of *Dove* state that the cell bus (NOT the serial links) is clocked at 100 MHz without mentioning the clocking rate of either the serial links or the backplane. The Examiner's Answer asserts – with absolutely NO support from the cited reference – that it is "obvious" that the "serial links" 550 and the backplane must operated at the same clock rate of 100 MHz. As previously noted, link 550 is NOT a serial link. In addition, the backplane and the serial links need not, necessarily, be operated at the same clock rate to achieve the targeted through-put: the backplane could be operated at a higher clock rate (e.g., some multiple of the clock rate employed for the serial links).

With regard to the recitation that the high speed serial link clock rate is 65.536 MHz in claim 15 and the recitation that the high speed serial link serialization/deserialization devices both (a) multiply the link clock rate by a factor of 20 and (b) 8B/10B encode in claim 16, the Examiner's Answer asserts that Applicant must prove a new or unexpected benefit. Examiner's Answer, page 27. Such assertion is improper under the *prima facie* burden required for obviousness rejections.

CONCLUSION

The cited references, taken alone or in combination, fail to disclose every limitation of the claimed invention. Therefore, the rejections of claims 10–13 and 17 under 35 U.S.C. § 102(e) and of claims 1–9, 14–16 and 18–19 under 35 U.S.C. § 103 are improper. Applicant respectfully

requests that the Board of Appeals reverse the decision of the Examiner below rejecting pending claims 1–20 in this application.

Respectfully submitted,

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